Dean Michael B Ancajas

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Qualification Summary

- Five (5) years research experience in Computer Architecture with publications in prestigious conferences.
- Two (2) years experience in workload analysis of various benchmarks to guide architectural designs.
- Experienced in performance/power modeling and design space exploration using full-system architectural simulators (Gem5, Gems/Garnet, PTLsim, DRAMSim2, MS2Sim).
- Proficient in the use of batch job scheduling to run hundreds of architectural simulations in a clustered linux environment.

Awards and Scholarships

- **Best Paper Award** International Conference on Computer Design (ICCD) 2012 (5 out of 250+)
- **Outstanding Graduate Research Assistant** Utah State University, ECE Department, 2013
- **Vice-Presidential Research Fellowship** Utah State University, 2010-2011
- **2nd Place Programming Contest** Utah State University, 2011
- **Faculty Research Incentive Award** UP Diliman, 2010
- **Graduate Scholar** Department of Science and Technology (NSF equivalent), 2007-2009
- **Undergraduate Scholar** Megaworld Foundation, 2002-2007

Education

PhD Electrical Engineering (Computer Architecture), Fall 2010-Spring 2014, GPA: **4.0/4.0**
Utah State University, Logan, Utah, USA
MS Electrical Engineering (Computer Architecture) October 2010, GPA: **4.0/4.0**
University of the Philippines, Quezon City, PH
BS Computer Engineering (Rank #3 in program) April 2007
University of the Philippines, Quezon City, PH

Research Experience

Utah State University, Logan, Utah

Graduate Research Assistant, BRIDGE Lab Advisor: Dr. Koushik Chakraborty (Fall 2010-Present)

Dynamic Memory Relocation for 3D Multicores:

- Designed memory mapping techniques to exploit locality in 3D multicore designs.
- Did workload analysis of parallel and multiprogram workloads to profile the memory access distribution throughout different DRAM banks.
- Interfaced a cycle-accurate DRAM model to a processor simulator to accurately model the memory system.
- Evaluated proposed techniques' performance and power using a cycle-accurate full-system simulator
- Constructed workload infrastructure for use in research group.
- Published at Design Automation Conference 2013 (DAC 2013).

Architectures for Reliable On-Chip Networks:

- Did workload analysis of the cache communication traffic of a 16-core system to classify traffic importance.
- Workload analysis of the bit patterns of cache communication traffic of a 64-core system to measure Hot Carrier Injection impact of a benchmark.
- Proposed HCI and NBTI-tolerant architectural designs.
- Ran design space exploration using a full-system simulator to study the system performance impact of proposed designs.
- Two publications at DAC 2013 and Design, Automation and Test in Europe (DATE) Conference 2013.

NBTI Mitigation in the Physical Register File through Stress Prediction:

- Analyzed the stress impact of certain instructions on the physical registers.
- Studied different programming constructs that generate stress on the physical register file.
- Published and won Best Paper Award at ICCD 2012.

Efficiently Tolerating Timing Violations in Pipelined Microprocessors:

- Architectural redesign of a module that wakes up instructions in the Issue Queue to accomodate timing violation-awareness.
- Power evaluation of a timing violation-aware processor using the FabScalar framework.
- Published in DAC 2013

UP Diliman, Electrical and Electronics Engineering Institute

Graduate Research Assistant (June 2007 - Oct 2010)

- Explored the performance of different resource sharing algorithms for SMT processors using the PTLSim full-system simulator.
- Taught classes, developed problem sets and exam questions for courses such as computer organization and programming fundamentals.

UP Diliman, Electrical and Electronics Engineering Institute

Undergraduate Research Assistant (Oct 2005 - June 2007)

- Implemented DLX RISC ISA in Verilog RTL with extensions for dual-core operation.
- Administrated 30+ linux laboratory computers.

Select Publications

- *DMR3D: Dynamic Memory Relocation in 3D Multicore Systems.* **Ancajas D.M.**, Chakraborty K., Roy S. Design Automation Conference 2013 (DAC 2013). Austin, Texas.
- *HCI Tolerant Network-on-Chip Router Microarchitecture.* **Ancajas D.M.**, Nickerson J.M., Chakraborty K., Roy S. Design Automation Conference 2013 (DAC 2013). Austin, Texas.
- *Efficiently Tolerating Timing Violations in Pipelined Microprocessors.* Chakraborty K., Cozzens B., Roy S., **Ancajas D.M.** Design Automation Conference 2013 (DAC 2013). Austin, Texas.
- *Proactive Aging Management on Heterogeneous Network-On-Chips.* **Ancajas D.M.**, Chakraborty K., Roy S. Design Automation and Test in Europe Conference 2013 (DATE 2013). Grenoble, France.
- *Mitigating NBTI in the Physical Register File through Stress Prediction.* (Best Paper Award). Kothawade S., **Ancajas D.M.**, Chakraborty K., Roy S. International Conference on Computer Design 2012 (ICCD 2012). Quebec, Canada.
- *Exploring High-Throughput Computing Paradigm for Global Routing*. Han Y., **Ancajas D.M.**, Chakraborty K., Roy S. IEEE Transactions on Very Large Scale Integration (TVLSI 2012).
- *Exploring High-Throughput Computing for Global Routing*. Han Y., **Ancajas D.M.**, Chakraborty K., Roy S. International Conference on Computer Aided Design 2011 (ICCAD 2011). San Jose, CA.
- *Dual Core Capability of a 32-bit DLX Microprocessor*. **Ancajas D.M.**, *et. al*. IEEE Region 10 Conference 2007. Taipei, Taiwan

Skills

- Programming Languages: C, C++, Verilog
- Architectural Simulators: Gem5, GEMS/Garnet, Booksim, DRAMSim2, MS2Sim
- Scripting: Ruby, BASH, awk
- Batch Scheduling: Condor

Activities

- External Reviewer for ISQED 2012 Conference

Relevant Coursework

- Computer Architecture, Parallel Computer Architecture, VLSI Design, Digital System Design, Computer Organization